

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 3 and 18 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first logic circuit comprising one or more saturation counters and configured to synchronize a plurality of input clock signals; and

5 a second logic circuit configured to detect and present a faster clock signal of said synchronized clock signals.

2. (ORIGINAL) The apparatus according to claim 1, wherein said first logic circuit comprises digital fast clock detection circuit.

3. (CANCELED)

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said second logic circuit comprises:

a fast clock detect circuit with programmable resolution configured to control a resolution of said apparatus.

5. (ORIGINAL) The apparatus according to claim 4, wherein said fast clock detect circuit is enabled or disabled in response to one or more configuration bits.

6. (ORIGINAL) The apparatus according to claim 5, wherein said fast clock detect logic, when disabled, is configured to be by-passed by a programmable configuration bit.

7. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to synchronously select said faster clock signal.

8. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is fully configurable.

9. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to provide programmable resolution.

10. (ORIGINAL) The apparatus according to claim 9, wherein said programmable resolution is configured to be increased or decreased by adjusting a count value.

11. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to provide automatic detection and configuration of one or more devices to said faster clock signal.

12. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to control one or more first-in first-out (FIFO) memories using a single port memory.

13. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to control one or more multiqueue memories using a single port memory.

14. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to control one or more multiport memories using a single port memory.

15. (ORIGINAL) The apparatus according to claim 1, wherein:

said first logic circuit comprises a faster clock detect circuit configured to synchronize said plurality of input clock
5 signals; and

said second logic circuit comprises a configuration resolution circuit configured to control a resolution of said

apparatus, a configuration circuit configured to control a selection of said faster clock signal and a select circuit
10 configured to select said faster clock signal.

16. (CURRENTLY AMENDED) An apparatus comprising:

means for synchronizing a plurality of input clock signals with one or more counters; ~~and~~

means for detecting and presenting a faster clock signal
5 of said synchronized clock signals; and

means for controlling resolution in response to one or more configuration bits.

17. (CURRENTLY AMENDED) A method for selecting a clock signal, comprising the steps of:

(A) synchronizing a plurality of input clock signals with one or more counters; ~~and~~

5 (B) detecting and presenting the faster clock signal of said synchronized clock signals; and

(C) controlling resolution in response to one or more configuration bits.

18. (CANCELED)

19. (NEW) An apparatus comprising:

a first logic circuit comprising one or more counters and configured to synchronize a plurality of input clock signals; and

a second logic circuit configured to detect and present a faster clock signal of said synchronized clock signals, wherein

5 said second logic circuit comprises a fast clock detect circuit (i) with programmable resolution configured to control a resolution of said apparatus and (ii) enabled or disabled in response to one or more configuration bits.